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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/682,134	10/09/2003	David Arnold Luick	ROC920020127US1	1346

46296 7590 01/20/2006

MARTIN & ASSOCIATES, LLC
P.O. BOX 548
CARTHAGE, MO 64836-0548

EXAMINER	
MEONSKE, TONIA L	
ART UNIT	**PAPER NUMBER**
2181	

DATE MAILED: 01/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/682,134	LUICK, DAVID ARNOLD	
	Examiner	Art Unit	
	Tonia L. Meonske	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-22 have been examined

Specification

2. The specification is objected to for improper arrangement. The following guidelines illustrate the preferred layout for the specification of a utility application. These guidelines are suggested for the applicant's use.

Arrangement of the Specification

As provided in 37 CFR 1.77(b), the specification of a utility application should include the following sections in order. Each of the lettered items should appear in upper case, without underlining or bold type, as a section heading. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

(a) TITLE OF THE INVENTION.
(b) CROSS-REFERENCE TO RELATED APPLICATIONS.
(c) STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT.
(d) THE NAMES OF THE PARTIES TO A JOINT RESEARCH AGREEMENT
(e) INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC (See 37 CFR 1.52(e)(5) and MPEP 608.05. Computer program listings (37 CFR 1.96(c)), "Sequence Listings" (37 CFR 1.821(c)), and tables having more than 50 pages of text are permitted to be submitted on compact discs.) or
REFERENCE TO A "MICROFICHE APPENDIX" (See MPEP § 608.05(a). "Microfiche Appendices" were accepted by the Office until March 1, 2001.)
(f) BACKGROUND OF THE INVENTION.
(1) Field of the Invention.
(2) Description of Related Art including information disclosed under 37 CFR 1.97 and 1.98.
(g) BRIEF SUMMARY OF THE INVENTION.
(h) BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S).
(i) DETAILED DESCRIPTION OF THE INVENTION.
(j) CLAIM OR CLAIMS (commencing on a separate sheet).
(k) ABSTRACT OF THE DISCLOSURE (commencing on a separate sheet).
(l) SEQUENCE LISTING (See MPEP § 2424 and 37 CFR 1.821-1.825. A "Sequence Listing" is required on paper if the application discloses a nucleotide or amino acid sequence as defined in 37 CFR 1.821(a) and if the required "Sequence Listing" is not submitted as an electronic document on compact disc).

3. The following describes the content suggested for each section heading appearing in the specification.

Content of Specification

(a) Title of the Invention: See 37 CFR 1.72(a) and MPEP § 606. The title of the invention should be placed at the top of the first page of the specification unless the title is provided in an application data sheet. The title of the invention should be brief but technically accurate and descriptive, preferably from two to seven words may not contain more than 500 characters.

(b) Cross-References to Related Applications: See 37 CFR 1.78 and MPEP § 201.11.

(c) Statement Regarding Federally Sponsored Research and Development: See MPEP § 310.

(d) The Names Of The Parties To A Joint Research Agreement: See 37 CFR 1.71(g).

(e) Incorporation-By-Reference Of Material Submitted On a Compact Disc: The specification is required to include an incorporation-by-reference of electronic documents that are to become part of the permanent United States Patent and Trademark Office records in the file of a patent application. See 37 CFR 1.52(e) and MPEP § 608.05. Computer program listings (37 CFR 1.96(c)), "Sequence Listings" (37 CFR 1.821(c)), and tables having more than 50 pages of text were permitted as electronic documents on compact discs beginning on September 8, 2000.

Or alternatively, Reference to a "Microfiche Appendix": See MPEP § 608.05(a). "Microfiche Appendices" were accepted by the Office until March 1, 2001.

(f) Background of the Invention: See MPEP § 608.01(c). The specification should set forth the Background of the Invention in two parts:

(1) Field of the Invention: A statement of the field of art to which the invention pertains. This statement may include a paraphrasing of the applicable U.S. patent classification definitions of the subject matter of the claimed invention. This item may also be titled "Technical Field."

(2) Description of the Related Art including information disclosed under 37 CFR 1.97 and 37 CFR 1.98: A description of the related art known to the applicant and including, if applicable, references to specific related art and

problems involved in the prior art which are solved by the applicant's invention. This item may also be titled "Background Art."

(g) Brief Summary of the Invention: See MPEP § 608.01(d). A brief summary or general statement of the invention as set forth in 37 CFR 1.73. The summary is separate and distinct from the abstract and is directed toward the invention rather than the disclosure as a whole. The summary may point out the advantages of the invention or how it solves problems previously existent in the prior art (and preferably indicated in the Background of the Invention). In chemical cases it should point out in general terms the utility of the invention. If possible, the nature and gist of the invention or the inventive concept should be set forth. Objects of the invention should be treated briefly and only to the extent that they contribute to an understanding of the invention.

(h) Brief Description of the Several Views of the Drawing(s): See MPEP § 608.01(f). A reference to and brief description of the drawing(s) as set forth in 37 CFR 1.74.

(i) Detailed Description of the Invention: See MPEP § 608.01(g). A description of the preferred embodiment(s) of the invention as required in 37 CFR 1.71. The description should be as short and specific as is necessary to describe the invention adequately and accurately. Where elements or groups of elements, compounds, and processes, which are conventional and generally widely known in the field of the invention described and their exact nature or type is not necessary for an understanding and use of the invention by a person skilled in the art, they should not be described in detail. However, where particularly complicated subject matter is involved or where the elements, compounds, or processes may not be commonly or widely known in the field, the specification should refer to another patent or readily available publication which adequately describes the subject matter.

(j) Claim or Claims: See 37 CFR 1.75 and MPEP § 608.01(m). The claim or claims must commence on separate sheet or electronic page (37 CFR 1.52(b)(3)). Where a claim sets forth a plurality of elements or steps, each element or step of the claim should be separated by a line indentation. There may be plural indentations to further segregate subcombinations or related steps. See 37 CFR 1.75 and MPEP § 608.01(i)-(p).

(k) Abstract of the Disclosure: See MPEP § 608.01(f). A brief narrative of the disclosure as a whole in a single paragraph of 150 words or less commencing on a separate sheet following the claims. In an international application which has entered the national stage (37 CFR 1.491(b)), the applicant need not submit an abstract commencing on a separate sheet if an abstract was published with the international application under PCT Article 21. The abstract that appears on the cover page of the pamphlet published by the International Bureau (IB) of the

World Intellectual Property Organization (WIPO) is the abstract that will be used by the USPTO. See MPEP § 1893.03(e).

(l) Sequence Listing, See 37 CFR 1.821-1.825 and MPEP §§ 2421-2431. The requirement for a sequence listing applies to all sequences disclosed in a given application, whether the sequences are claimed or not. See MPEP § 2421.02.

Claim Objections

4. Claim 21 is objected to because of the following informalities: In line 2, the limitation "a plurality of secondary latched" appears to contain a typographical error. It appears that Applicant intended the limitation to read "a plurality of secondary latches", and as such this is how the claim is interpreted for examination purposes. Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Terizan, US Patent 4,831,623 (herein after referred to as Terizan).

7. Referring to claim 1, Terizan has taught an integrated circuit comprising:

a. a register file bit comprising:

i. a first latch having a data input and a data output (Figure 1, element 16b, Figure 1A, elements OP REG 0 and OP REG 1);

ii. a second latch having a data input and a data output (Figure 1, element 18b, Figure 1A, elements TEST REG 0 and TEST REG 1);

iii. a feedback path from the data output of the second latch to the data input of the first latch (Figures 1 and 1A, The path from element 18b to element 16b, including element 20b. The path from element TEST REG 0 to element OP REG 0, including element OP MUX 0. The path from element TEST REG 1 to element OP REG 1, including element OP MUX 1.); and

iv. a context switch mechanism that causes the data [on the data output of the first latch to be written to the second latch, and that causes the data on the data output of the second latch to be written to the first latch (abstract, Figures 1 and 1A, column 1, line 64-column 2, line 57, Operational data, 16b and OP REG 0, are swapped with test data, 18b and OP REG 1, respectively.).

8. Referring to claim 2, Terizan has taught the integrated circuit of claim 1 as described above, and wherein the context switch mechanism comprises a swap signal coupled to the first latch (Figure 1 and 1A, column 5, lines 1-10, OPER CLK and TEST CLK).

9. Referring to claim 3, Terizan has taught the integrated circuit of claim 1, as described above, and wherein the context switch mechanism comprises a delay element between the data output of the first latch and the data input of the second latch (Figure 1, element 22b, Figure 1A, elements TEST MUX 0 and TEST MUX 1).

10. Referring to claim 4. Terizan has taught the integrated circuit of claim 1, as described above, and wherein the context switch mechanism comprises a delay element in the feedback path (Figure 1, element 20b, Figure 1A, elements OP MUX 0 and TEST MUX 1).

11. Referring to claim 5, Terizan has taught the integrated circuit of claim 1, as described above, and wherein the context switch mechanism comprises at least one clock signal that

latches data on the data input of the first latch to the data output of the first latch (Figures 1 and 1A, OPER CLK) and at least one clock signal that latches data on the data input of the second latch to the data output of the second latch (Figures 1 and 1A, TEST CLK).

12. Referring to claim 6, Terizan has taught the integrated circuit of claim 1, as described above, and further comprising a plurality of write ports on the data input of the first latch (column 4, lines 19-21, OPI parallel inputs).

13. Referring to claim 7, Terizan has taught the integrated circuit of claim 1, as described above, and further comprising a plurality of read ports on the data output of the first latch (column 4, lines 21-22, OPO parallel outputs).

14. Referring to claim 8, Terizan has taught an integrated circuit comprising:

a. a register file bit comprising:

i. a first latch (Figure 1, element 16b, Figure 1A, elements OP REG 0 and OP REG 1) having a data input with a plurality of write ports (column 4, lines 19-21, OPI parallel inputs) and a data output with a plurality of read ports (column 4, lines 21-22, OPO parallel outputs);

ii. a second latch having a data input and a data output (Figure 1, element 18b, Figure 1A, elements TEST REG 0 and TEST REG 1), wherein the data output of the first latch is coupled to the data input of the second latch through a first delay element (Figures 1 and 1A, The output of 16b is coupled to the input of 18b through element 22b. The output of OP REG 0 is coupled to the input of TEST REG 0 through TEST MUX 0. The output of OP REG 1 is coupled to the input of TEST REG 1 through TEST MUX 1.);

iii. a feedback path from the data output of the second latch to the data input of the first latch (Figures 1 and 1A, The path from 18b to 16b through 20b. The path from TEST REG 0 to OP REG 0 through OP MUX 0. The path from TEST REG 1 to OP REG 1 through OP MUX 1.), the feedback path including a second delay element (Figure 1 and 1A, element 20b, OP MUX 0 and OP MUX 1); and

iv. a swap signal coupled to the first latch that causes the data on the data output of the first latch to be written to the second latch, and that causes the data on the data output of the second latch to be written to the first latch (Figures 1 and 1A, OPER CLK and TEST CLK, abstract, column 1, line 64-column 2, line 57, Operational data, 16b, OP REG 0 and OP REG 0, are swapped with test data, 18b, OP REG 1 and OP REG 1, respectively.).

15. Referring to claim 9, Terizan has taught an integrated circuit comprising:

a. a register file bit comprising:

i. a primary latch having a data input and a data output (Figure 1, element 16b, Figure 1A, OP REG 0 and OP REG 1);

ii. a plurality of secondary latches each having a data input and a data output (Figure 1A, TEST REG 0, TEST REG 1);

iii. a feedback path from the data output of the plurality of secondary latches to the data input of the first latch (Figure 1A, The path from TEST REG 0 to OP REG 0 through OP MUX 0. The path from TEST REG 1 to OP REG 1 through OP MUX 1), the feedback path including a data selection mechanism for selecting

one data output from the plurality of secondary latches to feed back to the data input of the first latch (FIGURE 1A, OP MUX 0, OP MUX 1); and

iv. a context switch mechanism that causes the data on the data output of the primary latch to be written to a selected one of the plurality of secondary latches, and that causes the data on the data output of the selected one secondary latch to be written to the primary latch (Figures 1 and 1A, OPER CLK and TEST CLK, abstract, column 1, line 64-column 2, line 57, Operational data, 16b, OP REG 0 and OP REG 0, are swapped with test data, 18b, OP REG 1 and OP REG 1, respectively.).

16. Referring to claim 10, Terizan has taught the integrated circuit of claim 9, as described above, and wherein the context switch mechanism comprises a swap signal coupled to the primary latch (Figures 1 and 1A, OPER CLK and TEST CLK).

17. Referring to claim 11, Terizan has taught the integrated circuit of claim 9, as described above, and wherein the context switch mechanism comprises a delay element between the data output of the primary latch and the data inputs of the plurality of secondary latches (Figure 1A, element TEST MUX 0 and TEST MUX 1).

18. Referring to claim 12, Terizan has taught the integrated circuit of claim 9, as described above, and wherein the context switch mechanism comprises a delay element in the feedback path (Figure 1A, OP MUX 0, OP MUX 1).

19. Referring to claim 13, Terizan has taught the integrated circuit of claim 9, as described above, and wherein the context switch mechanism comprises at least one clock signal that latches data on the data input of the primary latch to the data output of the primary latch and at

least one clock signal that latches data on the data input of a secondary latch to the data output of the secondary latch (Figure 1A, OPER CLK and TEST CLK).

20. Referring to claim 14, Terizan has taught the integrated circuit of claim 9, as described above, and further comprising a plurality of write ports on the data input of the primary latch (column 4, lines 19-21, OPI parallel inputs).

21. Referring to claim 15, Terizan has taught the integrated circuit of claim 9, as described above, and further comprising a plurality of read ports on the data output of the primary latch (column 4, lines 21-22, OPO parallel outputs).

22. Referring to claim 16, Terizan has taught a method for performing a fast context switch in a register file, the method comprising the steps of: (A) providing a register file bit that stores first and second bit values (Figurse 1 and 1A, elements 16 b and 18 b, OP REG 0, OP REG 1, TEST REG 0, TEST REG 1); (B) when a context switch is required, swapping the first and second bit values (Figures 1 and 1A, abstract, column 1, line 64-column 2, line 57, Operational data: 16b, OP REG 0 and OP REG 0, are swapped with test data: 18b, OP REG 1 and OP REG 1, respectively.).

23. Referring to claim 17, Terizan has taught the method of claim 16, as described above, and wherein the swapping of the first and second bit values occurs in a single clock cycle (column 5, lines 8-10).

24. Referring to claim 18, Terizan has taught the method of claim 16, as described above, and wherein the register file bit comprises a first latch that stores the first value (Figure 1, element 16b, Figure 1A, elements OP REG 0 and OP REG 1) and a second latch that stores the second value (Figure 1, element 18b, Figure 1A, elements TEST REG 0 and TEST REG 1), the first

latch including a plurality of write ports (column 4, lines 19-21, OPI parallel inputs) and a plurality of read ports (column 4, lines 21-22, OPO parallel outputs), the register file bit further including a feedback path that allows the first and second bit values in the first and second latches to be swapped (Figures 1 and 1A, The path from element 18b to element 16b, including element 20b. The path from element TEST REG 0 to element OP REG 0, including element OP MUX 0. The path from element TEST REG 1 to element OP REG 1, including element OP MUX 1, column 1, line 64-column 2, line 57).

25. Referring to claim 19, Terizan has taught a method for performing a fast context switch in a register file, the method comprising the steps of:

(A) storing a first value in a first latch of the register file (Figures 1 and 1A, element 16b, OP REG 0, and OP REG 1);

(B) moving the first value in the first latch to a second latch (abstract, column 1, line 64-column 2, line 57);

(C) storing a second value in the first latch of the register file (Figures 1 and 1A, element 18b, TEST REG 0, and TEST REG 1); and

(D) activating a context switch signal that causes the second value in the first latch to be stored in the second latch, and that causes the first value in the second latch to be stored in the first latch (Figures 1 and 1A, OPER CLK and TEST CLK, abstract, column 1, line 64-column 2, line 57, Operational data, 16b, OP REG 0 and OP REG 0, are swapped with test data, 18b, OP REG 1 and OP REG 1, respectively.).

26. Referring to claim 20, Terizan has taught the method of claim 19, as described above, and wherein the activation of the context switch signal in step (D) causes the context switch to occur in a single clock cycle (column 5, lines 8-10).

27. Referring to claim 21, Terizan has taught a method for performing a fast context switch in a register file that includes a primary latch (Figure 1, element 16b, Figure 1A, elements OP REG 0 and OP REG 1) and a plurality of secondary latched (Figure 1, element 18b, Figure 1A, elements TEST REG 0 and TEST REG 1), the method comprising the steps of:

(A) for each of the plurality of secondary latches, performing the steps of:

(A1) storing a value in the primary latch that corresponds to a selected thread

(A2) moving the value in the primary latch to a secondary latch (abstract, column 1, line 64-column 2, line 57);

(B) storing a value in the primary latch that corresponds to an active thread (abstract, column 1, line 64-column 2, line 57);

(C) selecting one of the secondary latches for performing a context switch with the primary latch (abstract, column 1, line 64-column 2, line 57, OP MUX 0 and OP MUX 1); and

(D) performing a context switch between the primary latch and the selected one secondary latch that causes the value in the primary latch to be stored in the selected one secondary latch (abstract, column 1, line 64-column 2, line 57), and that causes the value in the selected one secondary latch to be stored in the primary latch (abstract, column 1, line 64-column 2, line 57).

28. Referring to claim 22, Terizan has taught the method of claim 21, as described above, and wherein the context switch performed in step (D) occurs in a single clock cycle (column 5, lines 8-10).

Conclusion

29. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L. Meonske whose telephone number is (571) 272-4170. The examiner can normally be reached on Monday-Friday, with every other Friday off.

30. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on (571) 272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

31. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

tlm

/Henry Tsai/ 1/18/06

HENRY W. H. TSAI
PRIMARY EXAMINER